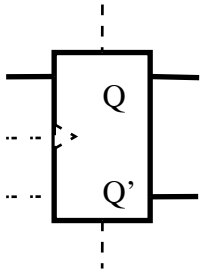
CPS311 - COMPUTER ORGANIZATION

Summary of latches and flip-flops

Basic Symbol for latches and flip-flops



- Outputs are always inverses
- One or two inputs (see behaviors below)
- Enable or clock not present on asynchronous type
- Level-triggered or master-slave may also have asynchronous preset and/or clear - often active low

Three basic types

Asynchronous (transparent) latch - Outputs change instantly when inputs changed
Synchronous (level triggered) latch - Has “enable” or “trigger”
- when inactive, inputs have no effect on outputs
- when active, outputs may change instantaneously when inputs changed
Master-slave - Has “clock”
- Outputs change on rising/falling edge of clock, based on inputs at that time

Historically, the term "flip-flop" has been used for all three. Some writers reserve the term only for synchronous devices or only for master-slave devices

Three kinds of behavior

S' R'	Q_{before}	Q_{after}
00	0	(disallowed)
00	1	(disallowed)
01	0	1
01	1	1
10	0	0
10	1	0
11	0	0 (no change)
11	1	1 (no change)

OR

SR	Q_{before}	Q_{after}
00	0	(no change)
00	1	(no change)
01	0	0
01	1	0
10	0	1
10	1	1
11	0	0 (disallowed)
11	1	1 (disallowed

(Asynchronous (transparent) latch, synchronous latch, or master-slave possible)

D	Q_{before}	Q_{after}
0	0	0
0	1	0
1	0	1
1	1	1

(Would be meaningless as asynchronous. Synchronous latch or master-slave possible. Asynchronous preset and/or clear often present as well)

JK	Q_{before}	Q_{after}
00	0	0 (no change)
00	1	1 (no change)
01	0	0
01	1	0
10	0	1
10	1	1
11	0	1
11	1	0

(Master-slave is only option. Asynchronous preset and/or clear often present as well)